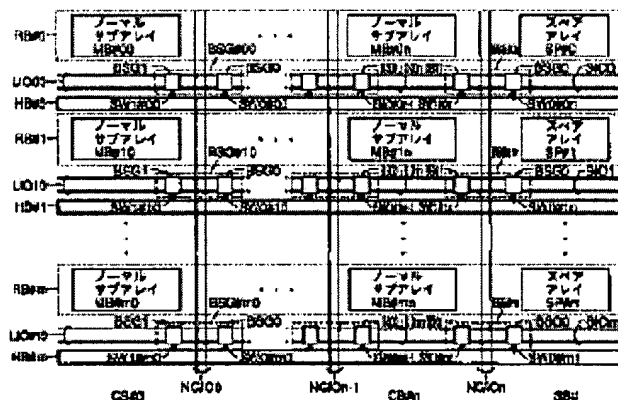# SEMICONDUCTOR MEMORY DEVICE

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Abstract of JP2000182390

PROBLEM TO BE SOLVED: To suppress the increase of a chip area by permitting an i-th connection circuit to output a control signal so that one of i-th to (i+n-m)-th local data buses is connected to an i-th global data bus and first to m-th global data buses are connected to m-pieces of local data buses. SOLUTION: Local data buses LIOi0-LIOin are installed in accordance with sub-arrays MB#i0-MB#in and a spare local data bus SIOi (i=0-m) is installed in accordance with a spare array SP#i. The local data buses LIOi0-LIOin transfer data only with the corresponding sub-arrays MB#i0-MB#in and the spare local data buses SIO0-SIOm with the corresponding spare arrays SP#0-SP#m. The spray arrays SP#i are installed in the plural normal sub-arrays MB#i0-MB#in in common so as to improve the use efficiency of a spare string.

PATENT ABSTRACTS OF JAPAN

(54) SEMICONDUCTOR MEMORY DEVICE

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